REMARKS/ARGUMENTS

Claims 1-20 are currently pending in the present patent application.

In an Office Action mailed on March 24, 2006, the Examiner rejected claims 12 and 13 under the 35 U.S.C. § 112 as failing to comply with the enablement requirement for including the term "ring." Referring to Figure 4 of the present application, a plurality of memory locations represented by the memory elements ELE[x]) contained in a plurality of subarrays are shown. Each sub-array includes serially coupled memory locations as illustrated. More specifically, each memory element ELE[x] is coupled to an adjacent memory element and the last or lowermost memory element is coupled back to the first or uppermost memory element of the sub-array in such a way to form a "loop" or a "ring." The use of the term "ring" in claims 12, 13 is clearly supported by this portion of the specification, along with others, such as the more detailed Figures 2A and 6 the associate descriptions. There is no requirement under U.S. patent law that specific terms used in the claims be contained in the specification. This rejection should be withdrawn.

In the Office Action, the Examiner rejected claims 8-10 and 14-16 under 35 U.S.C. § 102(e) as being anticipated by United States Patent Application Publication Number 2002/0087817 A1 to Tomaiuolo *et al.* ("Tomaiuolo"). Claim 8 recites a memory including a plurality of memory locations each having a contents and a control circuit coupled to the memory locations and operable to allow random access to the memory locations during a first mode of operation. The control circuit is also operable to allow sequential access to the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation.

In one embodiment covered by this claim, during a data storage operating mode sequential access to the contents of the memory elements ELE is provided via the uppermost element ELE[511] through a shift register type structure as depicted in Figure 3. Such sequential access could also be provided during a data retrieval operating mode. Regardless, access to the contents stored in the memory locations is provided "via a predetermined one of the memory locations."

Notwithstanding the examiner's assertions, the Tomaiuolo patent neither discloses nor suggests a memory as recited in claim 8. In Tomaiuolo, an interlaced memory structure is disclosed in which data may be randomly accessed in either an even matrix or an odd matrix during an asynchronous or random access mode of operation. When

consecutive memory address is applied to the memory are detected, the memory operates in an asynchronous or sequential mode of operation to sequentially access the contents of data stored in consecutive memory addresses contained within the even and odd matrices. Thus, even during the sequential mode a memory location corresponding to the next consecutive address is merely accessed and the contents of that memory location provided. The data is stored and even and odd matrices such that during the sequential mode the data accesses are interleaved, meaning that a first given address corresponds to an access of a member location in that even matrix, for example, while the next consecutive address or require an access to a memory location in the odd matrix.

With the structure of Tomaiuolo, the sequential access to the contents of the memory locations is not provided "via a predetermined one of the memory locations." Instead, as just described, with the system of Tomaiuolo sequential accesses merely correspond to alternately accessing corresponding memory locations in the even and odd matrices. Thus, sequential access is not provided through a predetermined one of the memory locations but instead through a plurality of memory locations corresponding to consecutive memory addresses. Moreover, while Tomaiuolo discloses one particular way of enabling a memory device to operate in sequential and random modes of operation, there is no suggestion of the approach set forth in the present application.

For these reasons, the combination of elements recited in claim 8 is allowable and dependent claims nine and 10 are allowable for at least the same reasons as claim eight and two to the additional limitations added by each of these claims. Claims 14-16 are allowable for similar reasons to those just described with reference to claim 1.

In the Office Action, the Examiner rejected claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,091,645 to Iadanza ("Iadanza") in view of Applicant Admitted Prior Art ("AAPA").

Claim 1 recites a memory including at least one array of memory elements, with the at least one array being partitioned into a plurality of sub-arrays of the memory elements. An array configuration circuit selectively puts the at least one array in one of two operating configurations. A first operating configuration is such that the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory. A second operating configuration is such that the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block, a data content of any memory element of the sub-

array being rotatable by shifts through the memory elements of the sub-array. A sub-array selector operates, responsive to a first memory address, selectings one among the at least two sub-arrays according to the first memory address and enabling access to the selected sub-array. A memory element access circuit operates, responsive to a second memory address, to enable access to a prescribed memory element in the selected sub-array after a prescribed number of shifts, depending on the second memory address, of the data content of the memory elements in the selected sub-array.

Even if Iadanza and the AAPA are combined, the structure recited in claim number one is not realized. Notwithstanding the Examiner's assertions, Iadanza does not disclose a structure for "data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array." can not be read in Iadanza, contrary to what the Examiner asserts. In fact, Iadanza discloses memory subarrays (12) including a plurality of memory cells (48) arranged in rows, with each row of memory cells that may have an associated row of transfer cells (50) for enabling movement of data vertically. This is different than recited in claim 1, wherein the rotating data among the memory elements of each sub-array when the second operating configuration is provided.

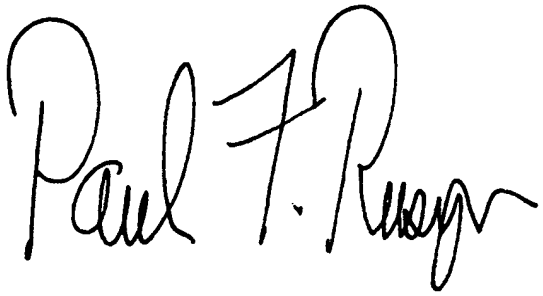
Furthermore, there is no motivation to combine Iadanza and the AAPA. The Examiner essentially argues that the prior existence of RAMs (see paragraph 7 of the present application) and of FIFOs (see paragraph 6) would have easily allowed a regular skilled technician to create a modification to the structure of Iadanza so as arrive at the invention of claim 1. Merely because two independent structures exist in the prior art does not mean that it would have been obvious to combine these structures. Indeed, if, as the Examiner states, Iadanza does not disclose the first and second operating configurations for the sub-arrays of the field programmable memory array, the prior knowledge of RAMs would merely suggest to an average skilled technician to configure the whole memory array of Iadanza in such a way that the memory locations are randomly accessible. On the other side, the prior knowledge of FIFOs (*i.e.*, of sequentially accessible memories) would merely suggest to an average skilled technician to configure the whole memory array of Iadanza in such a way that the memory locations are sequentially accessible (this is already envisaged in Iadanza, see for example the "physical LIFO/FIFO" embodiments described in the columns 10 and 11). However, in the claimed memory the sub-arrays can be put in either one of the two operating configurations, and this provides an efficient trade-off between random accessibility and access speed.

All remaining independent claims are allowable for reasons similar to those discussed above with reference to claims 1 and 8. All dependent claims not expressly mentioned above are allowable for at least the same reasons as the associated independent claim and do to the additional limitations added by each of these dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



Paul F. Rusyn
Registration No. 42,118
155 – 108th Avenue NE, Suite 350
Bellevue, WA 98004-5973
(425) 455-5575 Phone
(425) 455-5575 Fax